

Revision : 1.01

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[illegible]

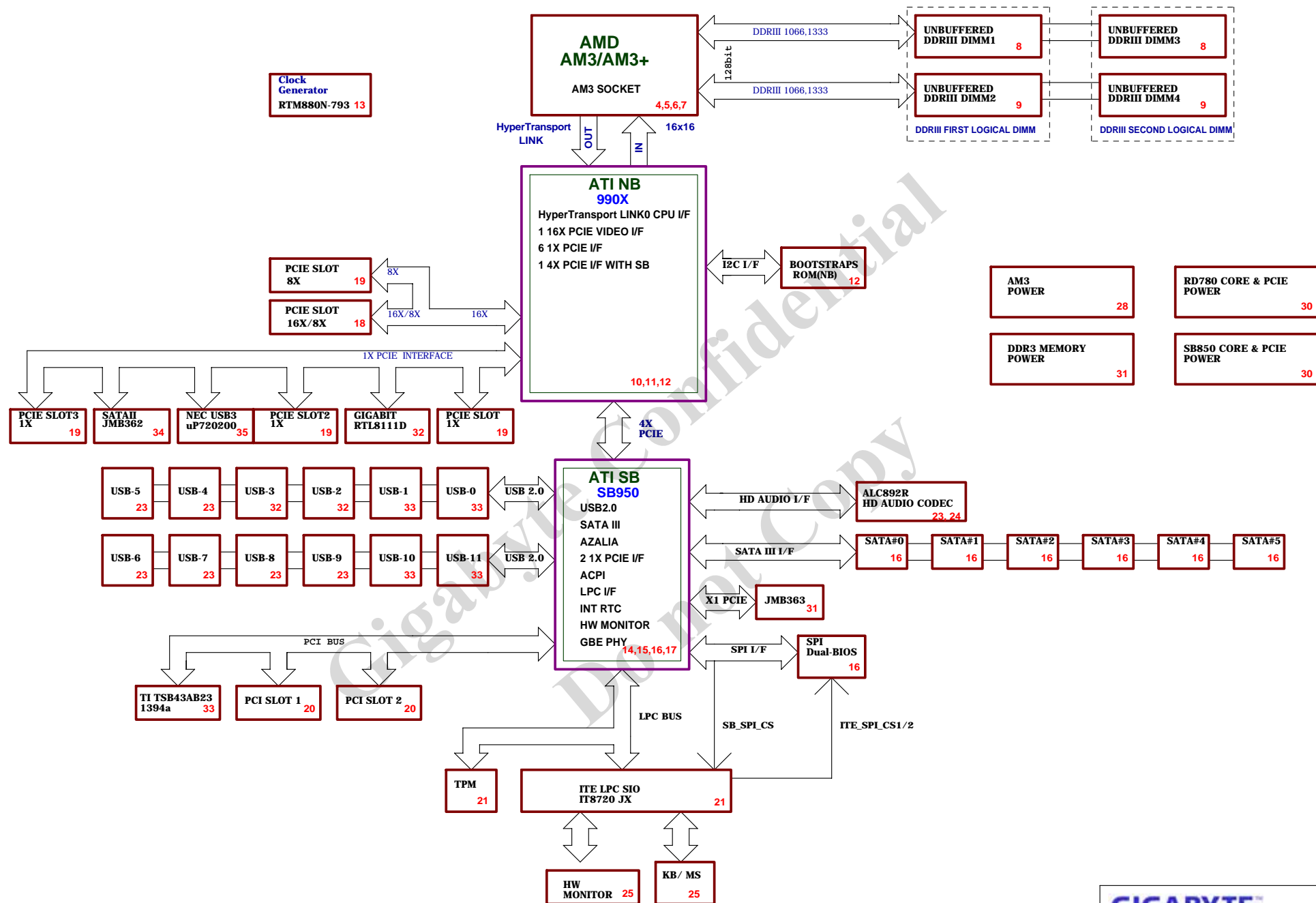
				
Title				
COVER SHEET				
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4 Layer, 4mil 50ohm +/- 15% L P-Code: U98094-0

Circuit or PCB layout change for next version

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Title			
BOM & PCB HISTORY			
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Title			
BLOCK DIAGRAM			
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L0_CADIN_L[0..15] <L0_CADIN_L[0..15] <10>
 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <10>
 L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <10>
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <10>

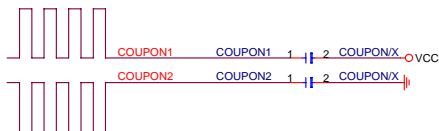
M2CPUA

HYPERTRANSPORT

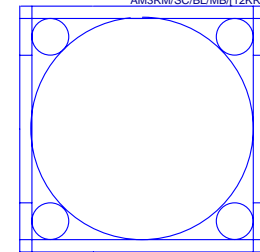
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<10> L0_CTLIN_H1	L0_CTLIN_H1 V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6 L0_CTLOUT_H1	>L0_CTLOUT_H1 <10>
<10> L0_CTLIN_L1	L0_CTLIN_L1 V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6 L0_CTLOUT_L1	>L0_CTLOUT_L1 <10>
<10> L0_CTLIN_H0	L0_CTLIN_H0 U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2 L0_CTLOUT_H0	>L0_CTLOUT_H0 <10>
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L0_CADIN_L15 V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4 L0_CADOUT_L15		
L0_CADIN_H14 T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6 L0_CADOUT_H14		
L0_CADIN_L14 T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6 L0_CADOUT_L14		
L0_CADIN_H13 R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5 L0_CADOUT_H13		
L0_CADIN_L13 T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4 L0_CADOUT_L13		
L0_CADIN_H12 P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6 L0_CADOUT_H12		
L0_CADIN_L12 P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6 L0_CADOUT_L12		
L0_CADIN_H11 M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6 L0_CADOUT_H11		
L0_CADIN_L11 M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6 L0_CADOUT_L11		
L0_CADIN_H10 L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5 L0_CADOUT_H10		
L0_CADIN_L10 M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4 L0_CADOUT_L10		
L0_CADIN_H9 K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6 L0_CADOUT_H9		
L0_CADIN_L9 K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6 L0_CADOUT_L9		
L0_CADIN_H8 J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5 L0_CADOUT_H8		
L0_CADIN_L8 K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4 L0_CADOUT_L8		
L0_CADIN_H7 U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1 L0_CADOUT_H7		
L0_CADIN_L7 U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1 L0_CADOUT_L7		
L0_CADIN_H6 R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2 L0_CADOUT_H6		
L0_CADIN_L6 T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3 L0_CADOUT_L6		
L0_CADIN_H5 R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1 L0_CADOUT_H5		
L0_CADIN_L5 R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1 L0_CADOUT_L5		
L0_CADIN_H4 N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2 L0_CADOUT_H4		
L0_CADIN_L4 P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3 L0_CADOUT_L4		
L0_CADIN_H3 L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2 L0_CADOUT_H3		
L0_CADIN_L3 M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3 L0_CADOUT_L3		
L0_CADIN_H2 L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1 L0_CADOUT_H2		
L0_CADIN_L2 L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AF1 L0_CADOUT_L2		
L0_CADIN_H1 J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2 L0_CADOUT_H1		
L0_CADIN_L1 K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3 L0_CADOUT_L1		
L0_CADIN_H0 J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1 L0_CADOUT_H0		
L0_CADIN_L0 J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1 L0_CADOUT_L0		

CPU-SK/941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

VLDT_A = VCC12_HT
 VLDT_B = HT12B

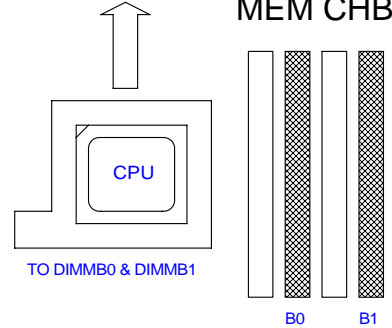
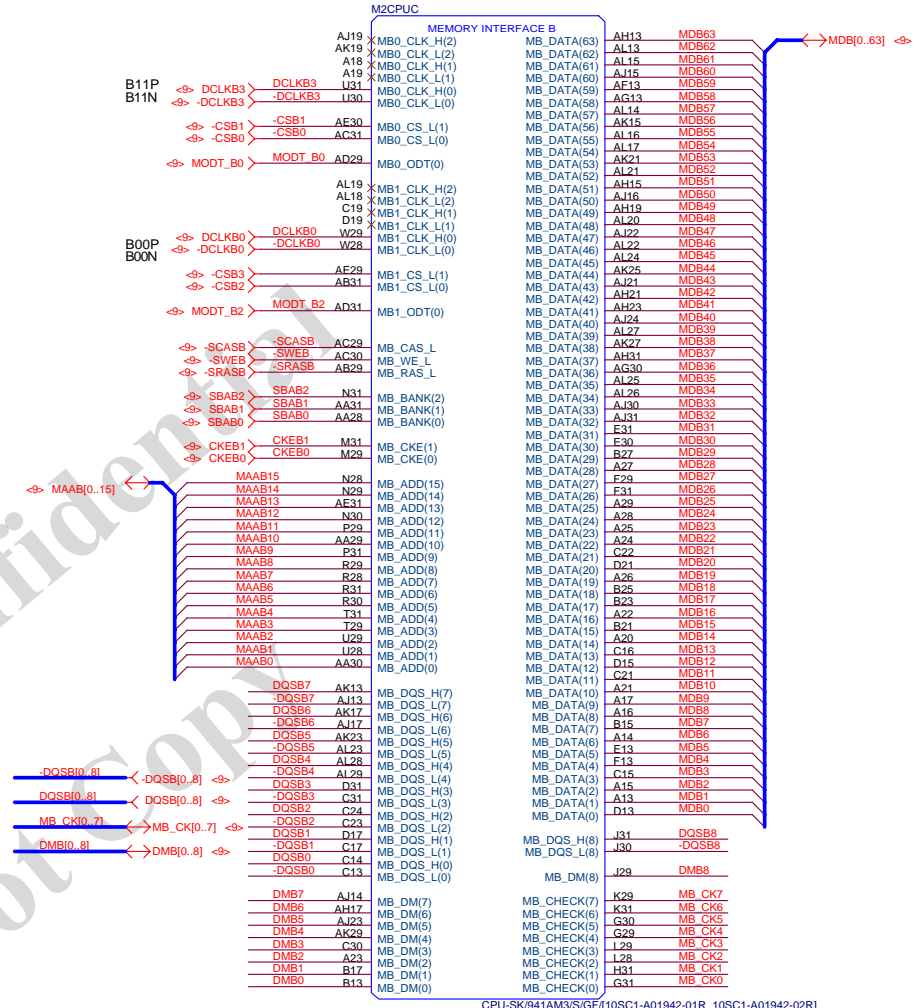


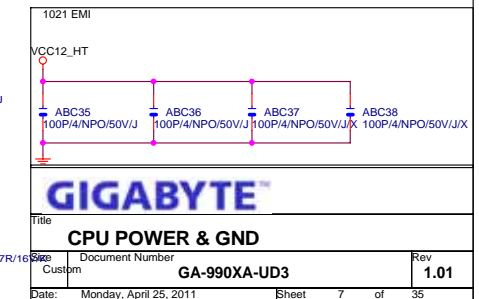
M2CPU
 AM3RM/SC/BL/MB/12KRC-04K812-21R_12KRC-04K812-22R]

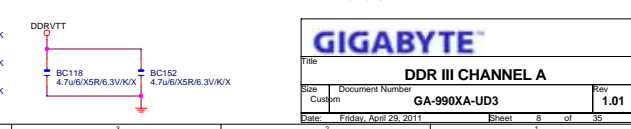
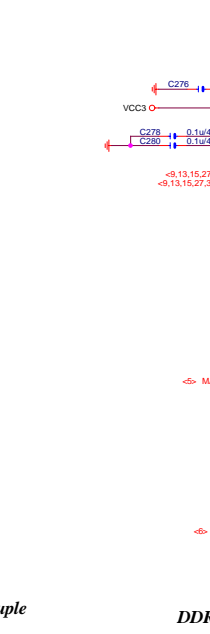
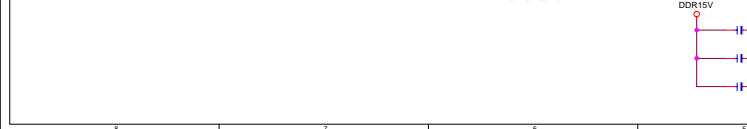


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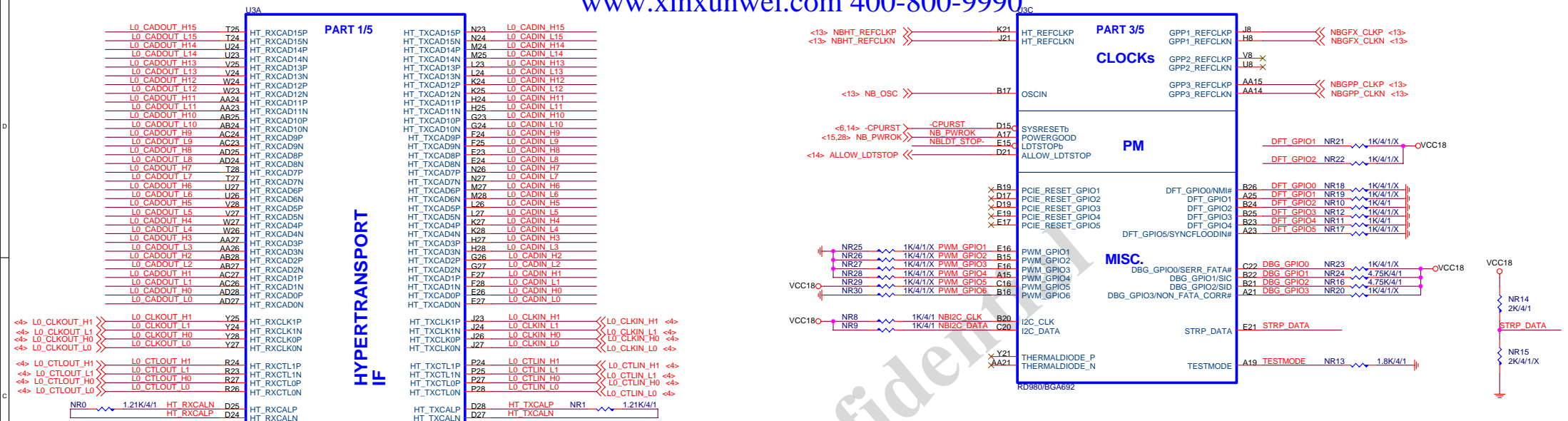
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CPU HYPER TRANSPORT			
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DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000: 4:2:4 B
001: 4:1:1:4 C
010: 1:1:1:1:1:4 L (Hardware Default)
011: 2:1:1:1:1:4 E
100: 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101: 01100
101: 01011

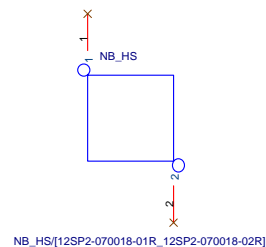
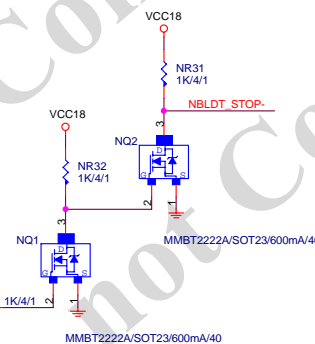
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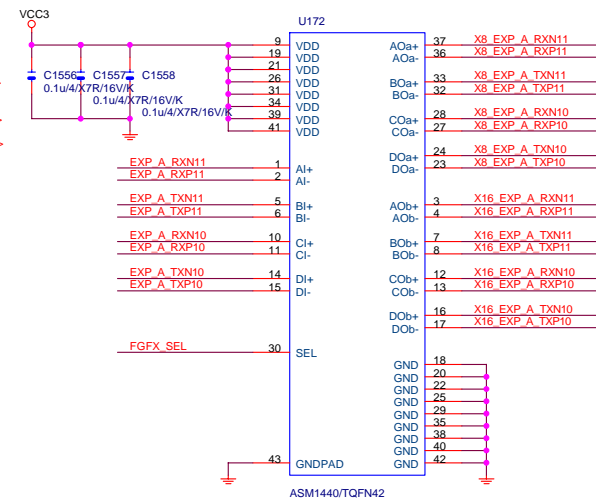
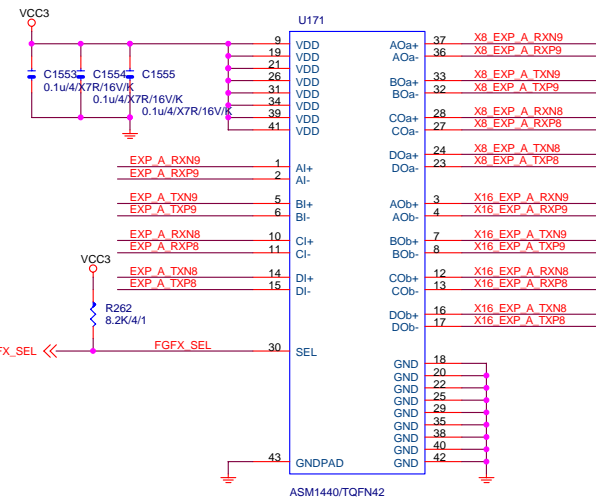
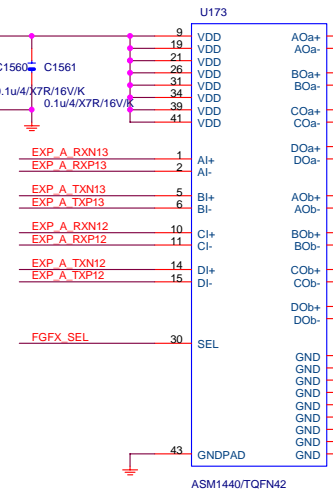
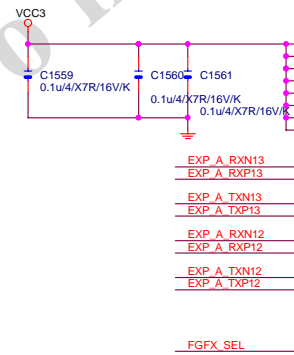
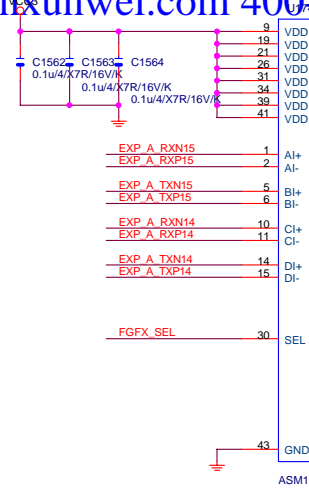
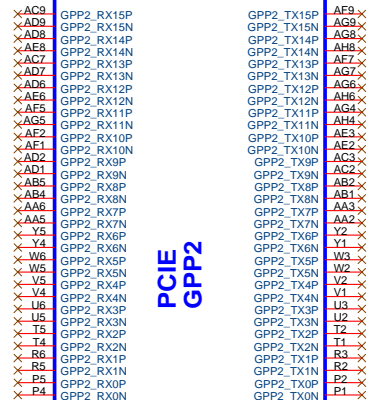
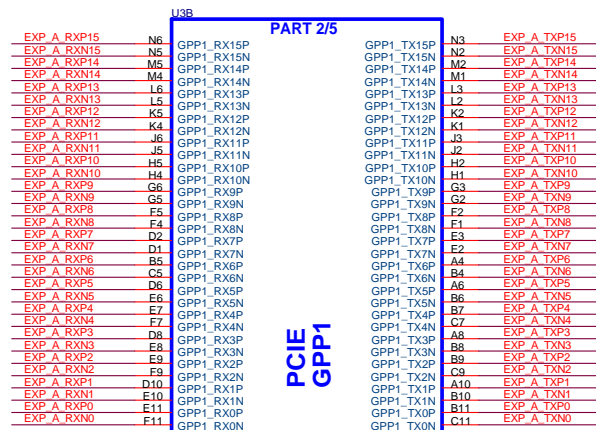
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable





Function	SEL
xI--> x0a	L (X8)
xI--> x0b	H (X16)

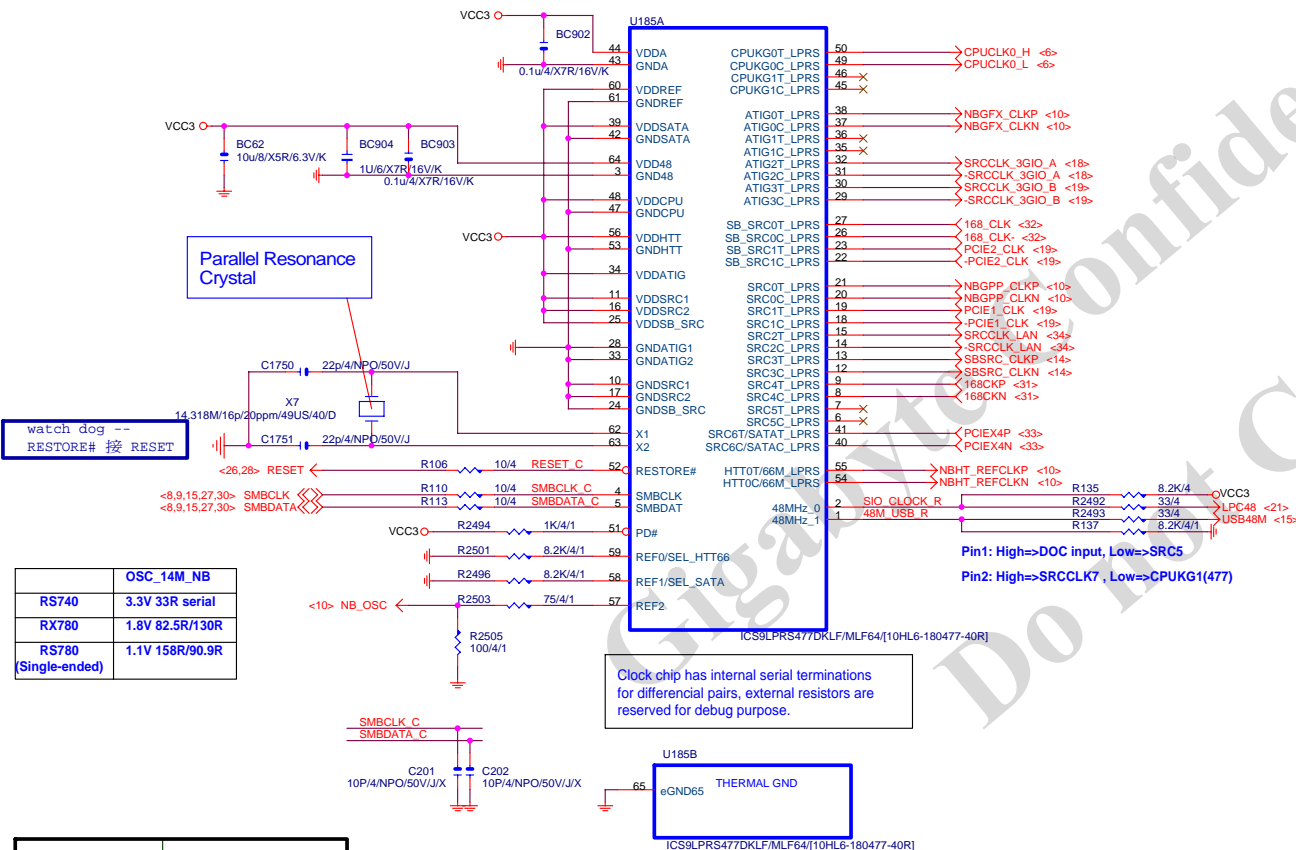


NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mills away from U800
 R851 less than 100 mills away from R800/801
 route CPU clock as 100ohm differential pair



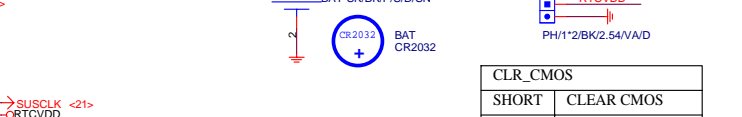
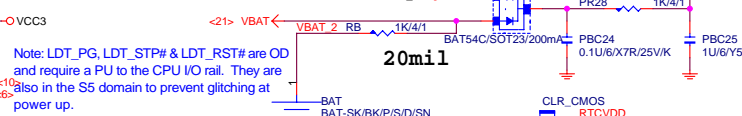
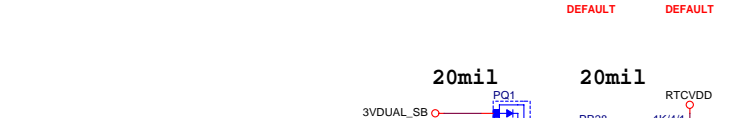
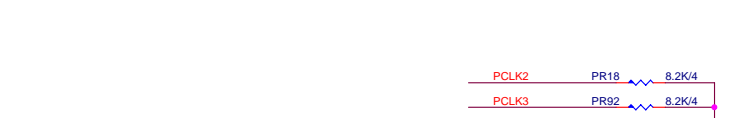
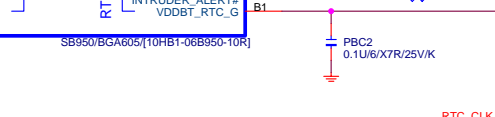
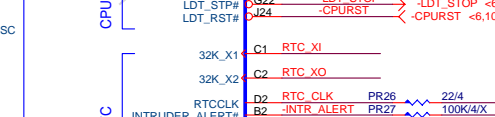
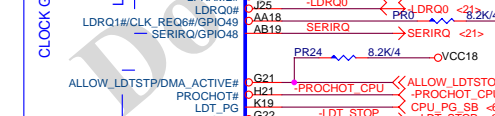
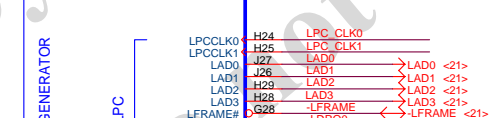
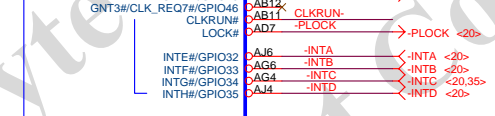
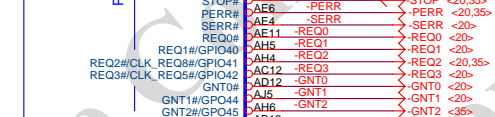
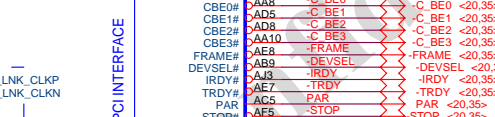
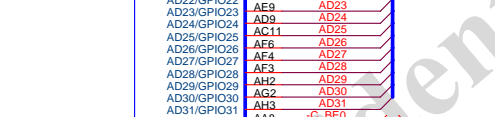
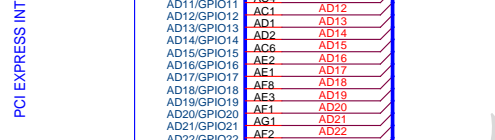
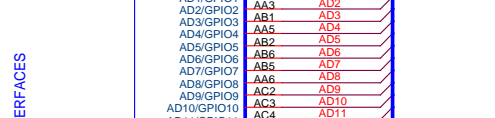
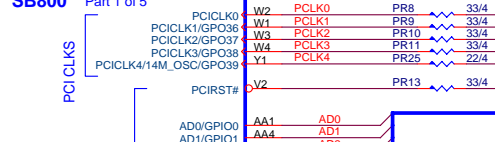
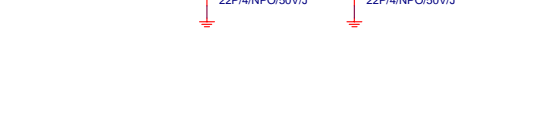
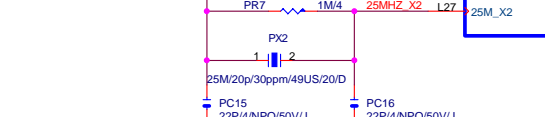
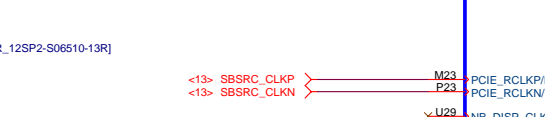
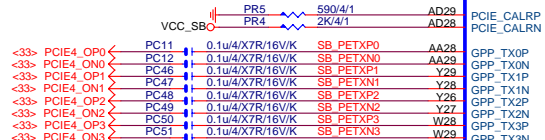
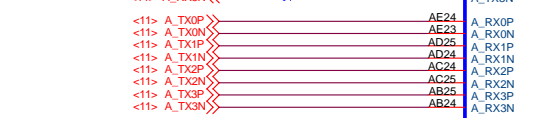
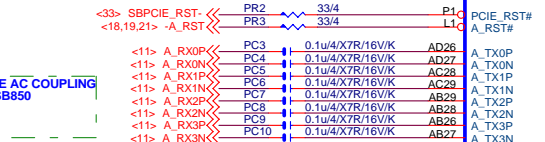
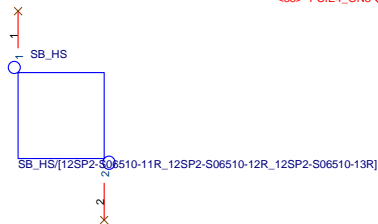
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Title			RTM880N-793		
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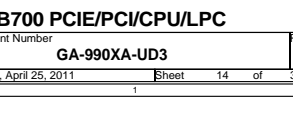
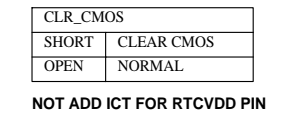
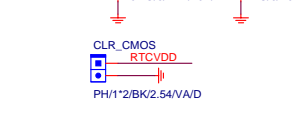
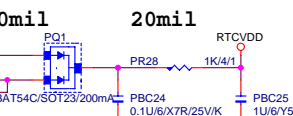
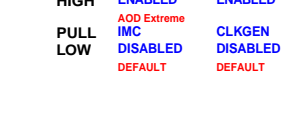
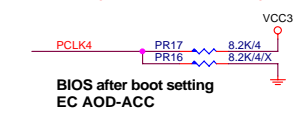
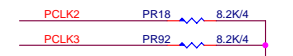


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK

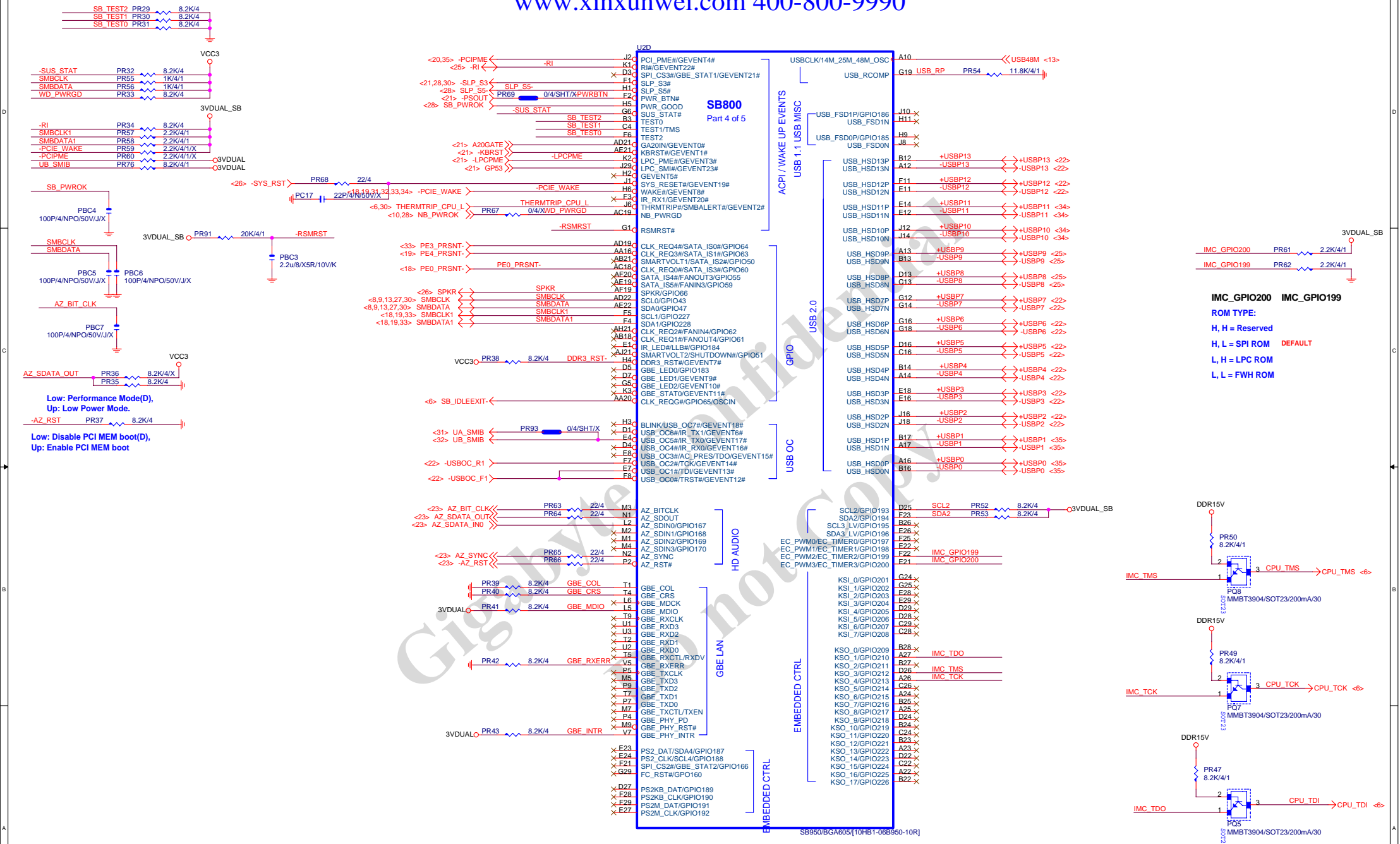


Low: Force PCIE GEN1, Up: Allow PCIE GEN2



GIGABYTE

Title		
ATI SB700 PCIE/PCI/CPU/LPC		
Size	Document Number	Rev
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PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

VCC_SBC

PR75

PR74

1K/4/1

SATA_CALRP

931/4/1

SATA_CALRN

AA14

SATA_CALRP

SATA_CALRN

AD11

SATA_ACT#/GPIO67

SATA_X1

AD16

SATA_X1

AC16

SATA_X2

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SATA_X2

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SATA_X2

SATA_X2

SATA_X2

SB SPI DI

PR70

22/4

SB SPI DI R

J5

SPI_DI/GPIO164

SPI_DO/GPIO163

SPI_CLK/GPIO162

SPI_CS1#/GPIO165

ROM_RST#/GPIO161

SPI ROM

SPI ROM

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SPI ROM



PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

SP TX0P C

PC18

0.01u/4/X7R/25V/K

SATA0TXPC

SATA0TXNC

SATA0RXNC

SATA0RXPNC

SATA0TXPC

SATA0TXNC

SATA0RXNC

SATA0RXPNC

SATA0TXPC

SATA0TXNC

SATA0RXNC

SATA0RXPNC

SATA0TXPC

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SATA0RXNC

SATA0RXPNC

SATA0TXPC

SATA0TXNC

SATA0RXNC

SATA0RXPNC

SATA0TXPC

SATA0TXNC

SATA0RXNC

SATA0RXPNC

SP TX2P C

PC22

0.01u/4/X7R/25V/K

SATA2TXPC

SATA2TXNC

SATA2RXNC

SATA2RXPNC

SATA2TXPC

SATA2TXNC

SATA2RXNC

SATA2RXPNC

SATA2TXPC

SATA2TXNC

SATA2RXNC

SATA2RXPNC

SATA2TXPC

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SATA2TXPC

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SATA2RXNC

SATA2RXPNC

SATA2TXPC

SATA2TXNC

SATA2RXNC

SATA2RXPNC

SP TX4P C

PC26

0.01u/4/X7R/25V/K

SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

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SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

SP RX4M C

PC28

0.01u/4/X7R/25V/K

SATA4RXNC

SATA4RXPNC

SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

SATA4TXPC

SATA4TXNC

SATA4RXNC

SATA4RXPNC

SATA4TXPC

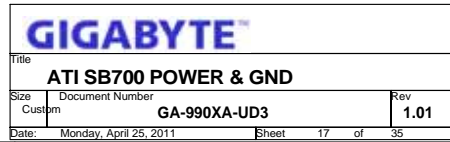
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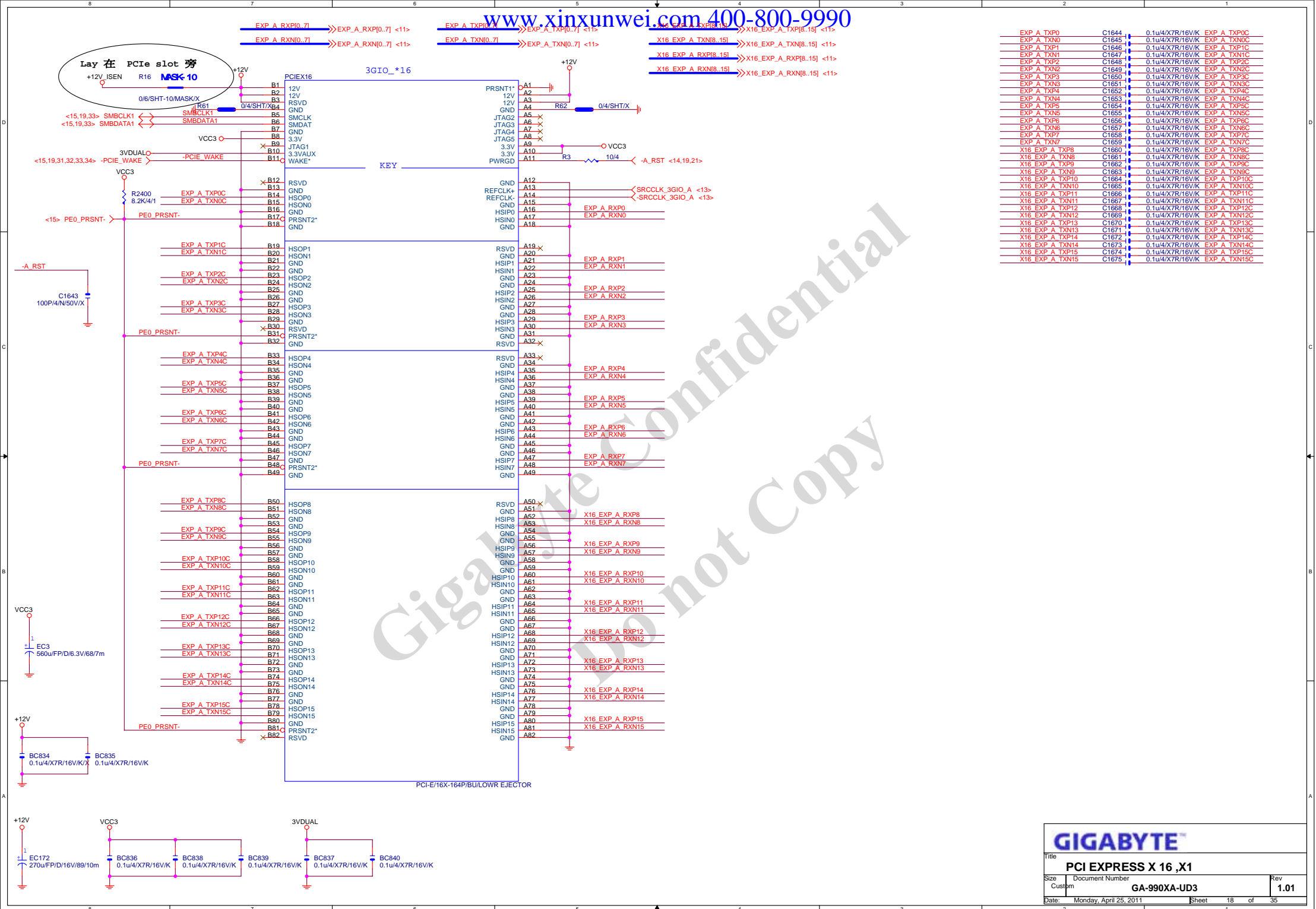
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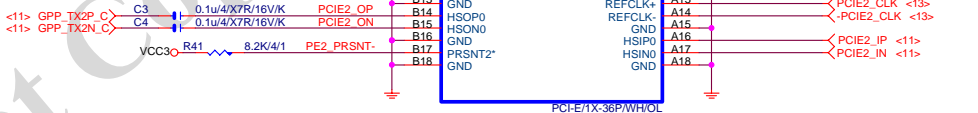
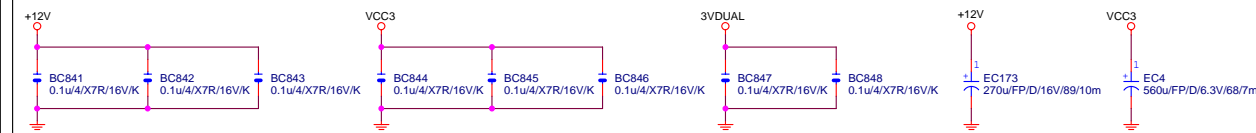
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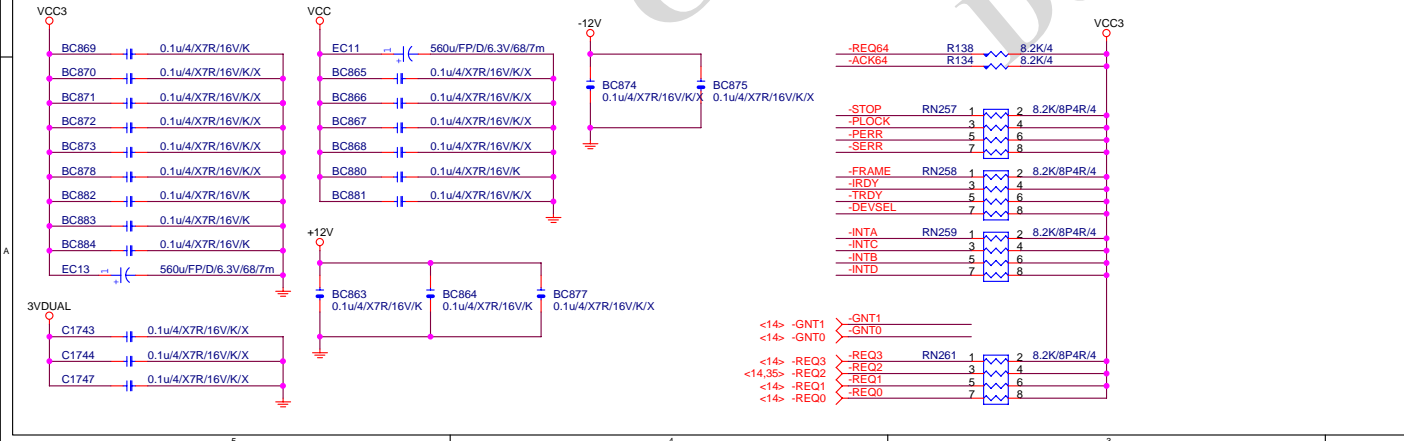
SATA4TXPC

SATA4TXNC

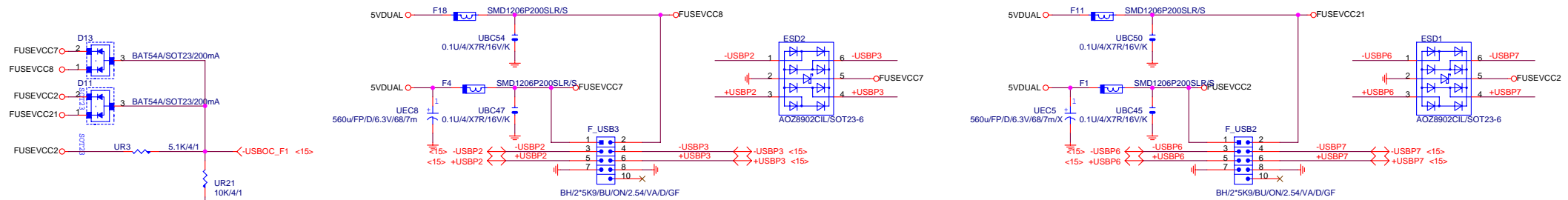




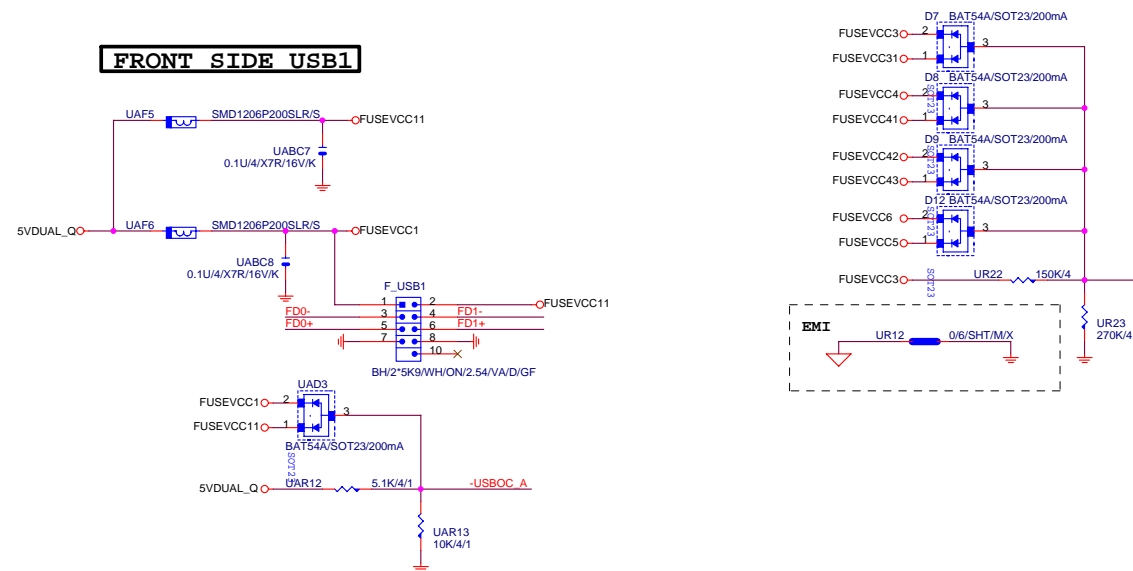




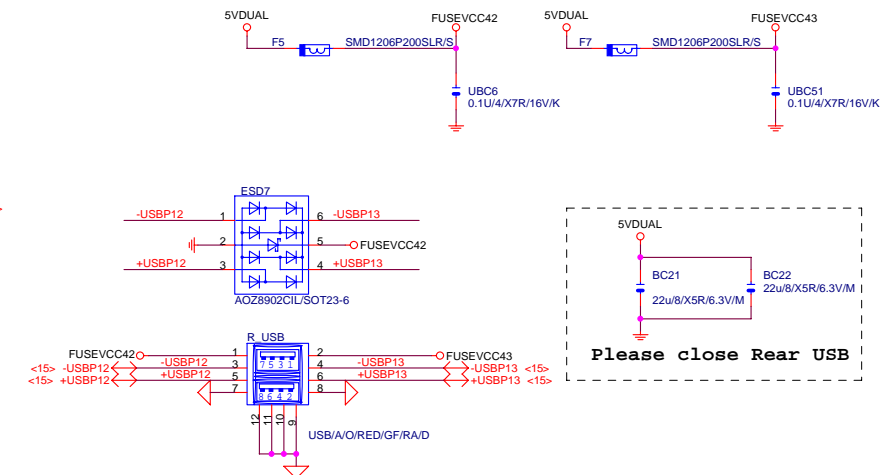
FRONT SIDE USB2



FRONT SIDE USB1

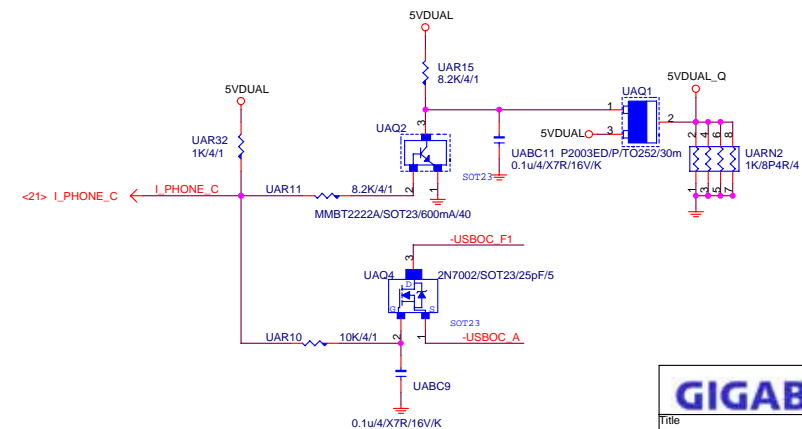
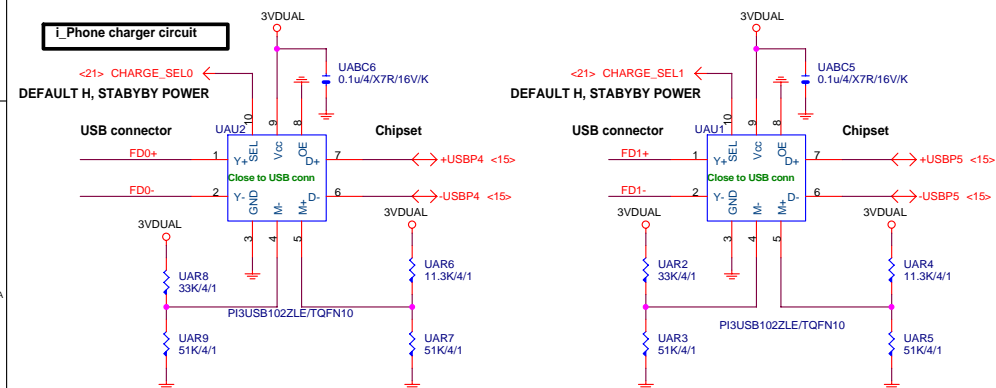


REAR USB



Please close Rear USB

I Phone charger circuit

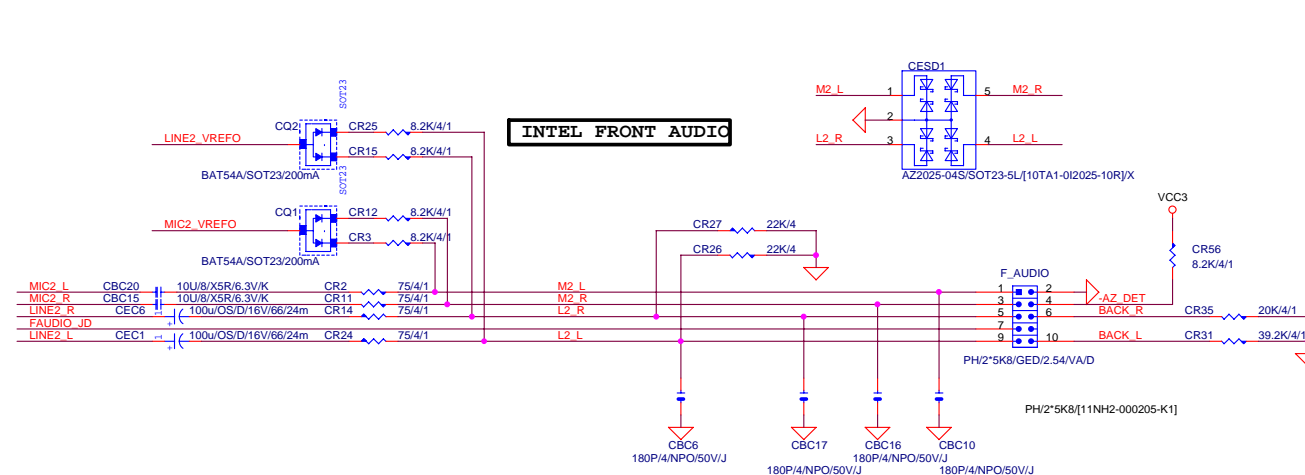
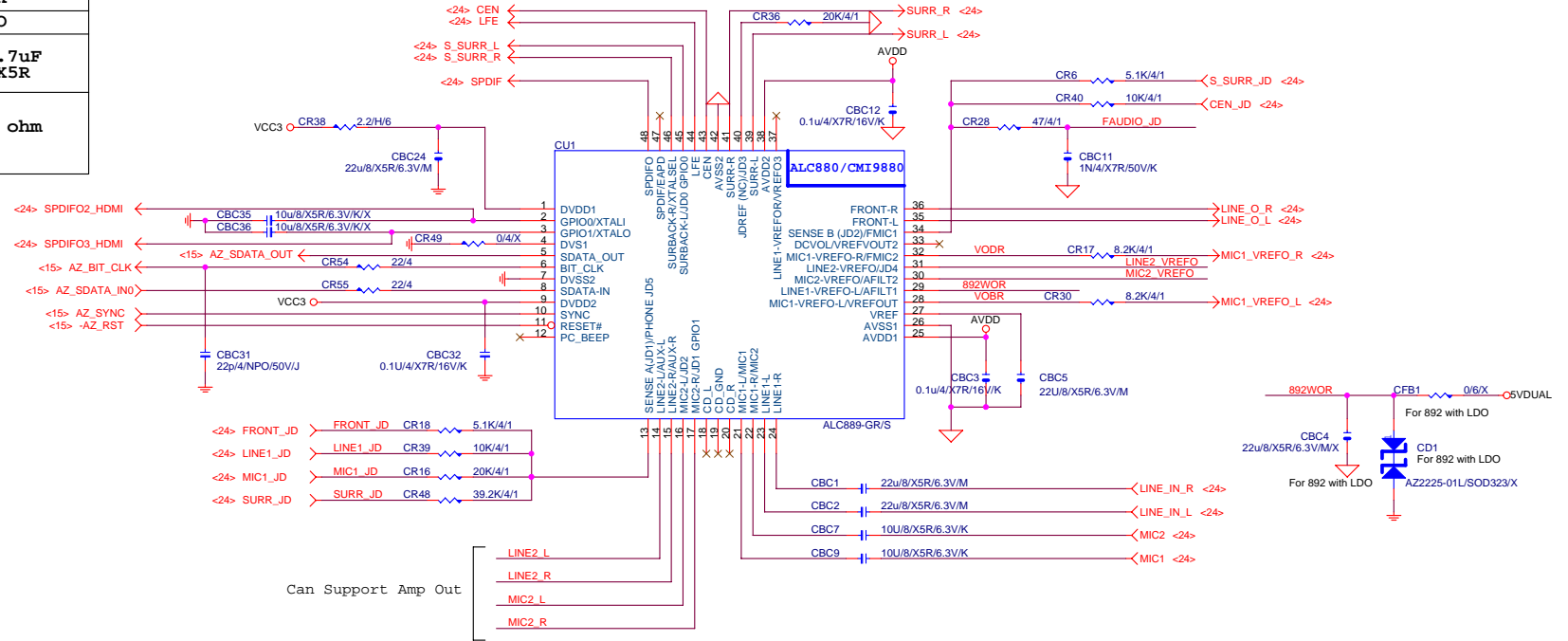


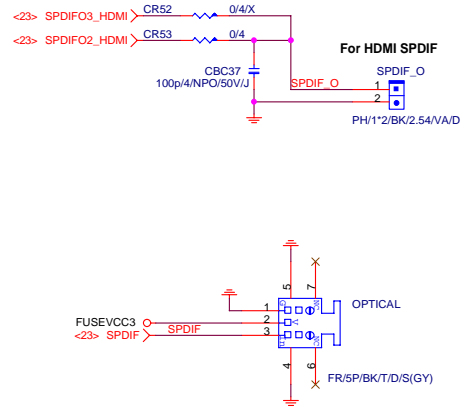
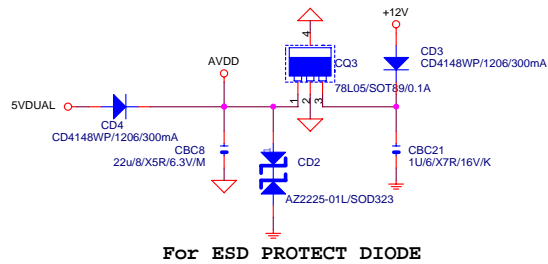
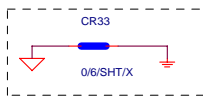
GIGABYTE®

COM/LPT/F_USB/I_PWR

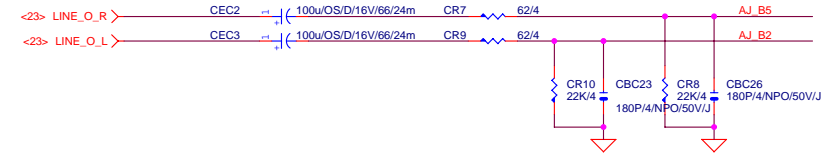
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	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm





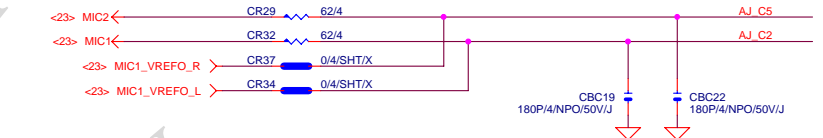
LINE OUT FRONT OUT



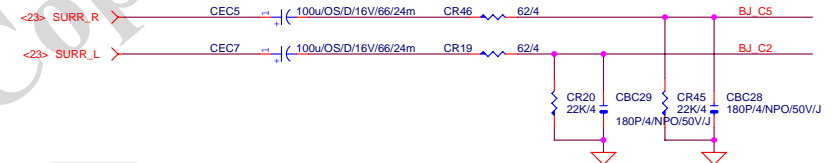
LINE-IN



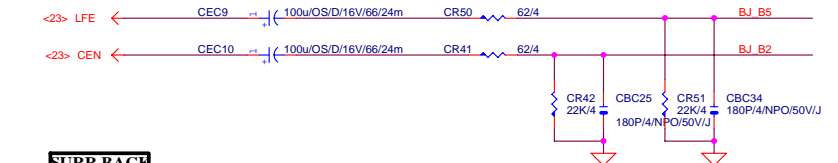
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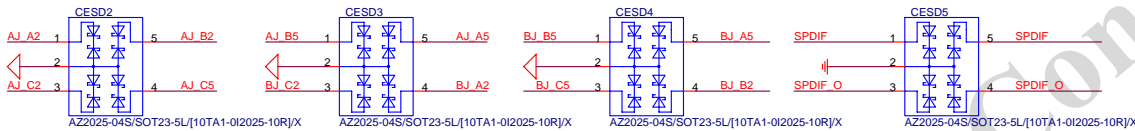
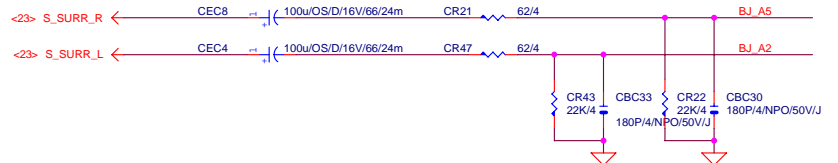
SURROUND



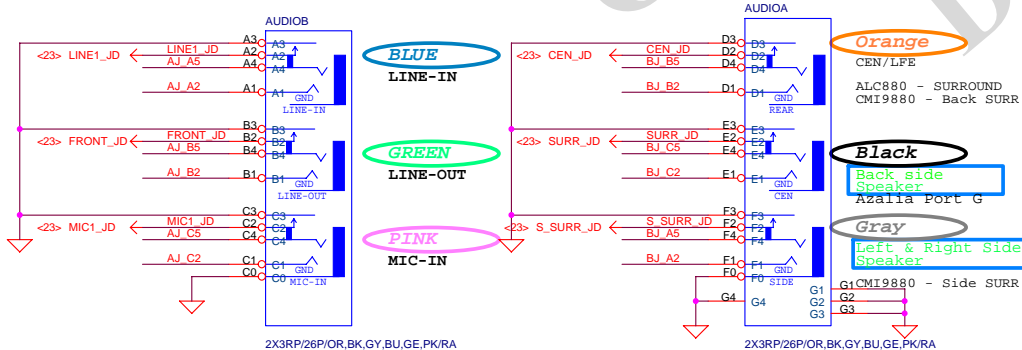
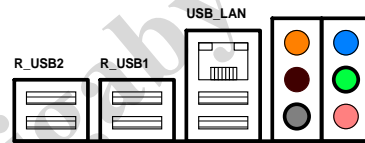
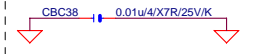
CEN/LFE



SURR BACK



For Audio precision test



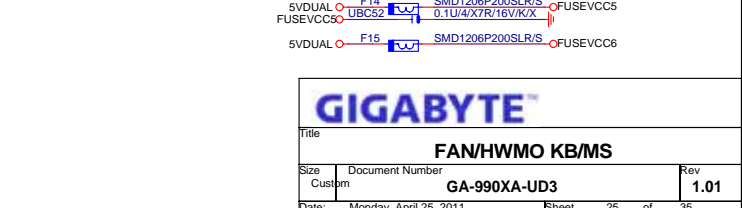
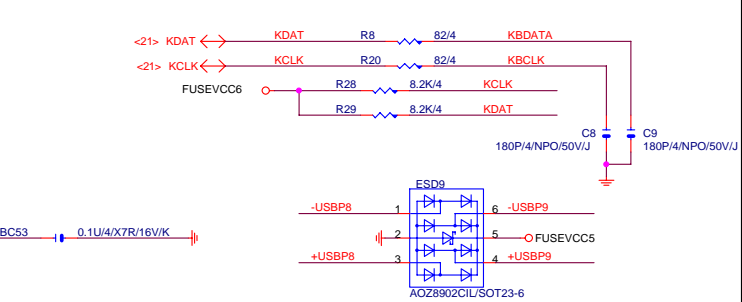
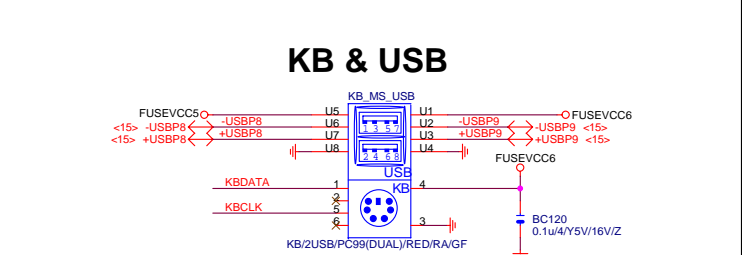
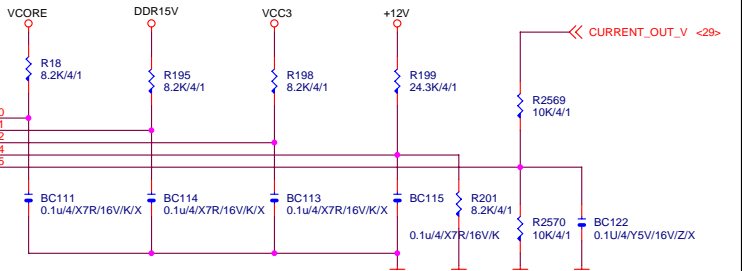
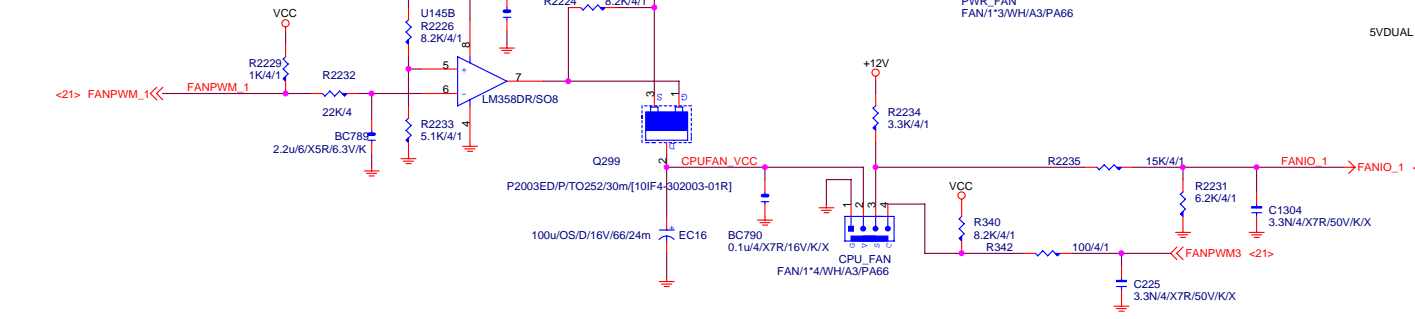
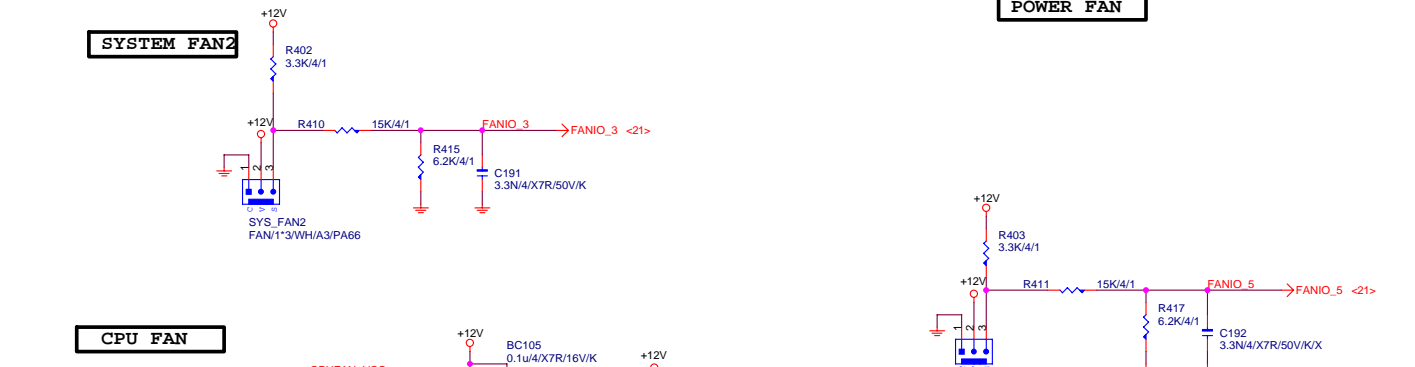
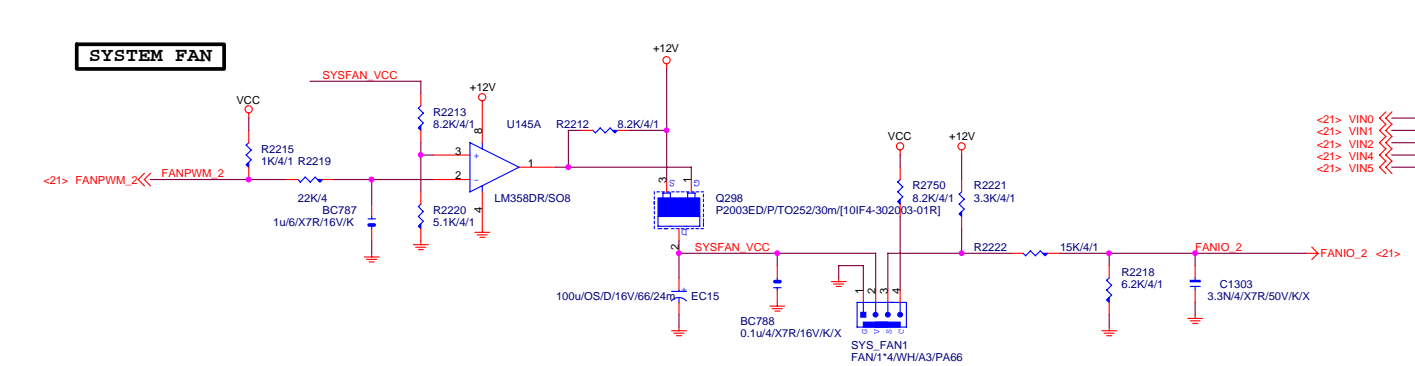
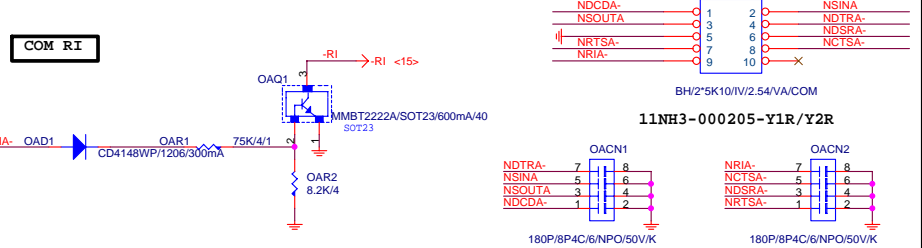
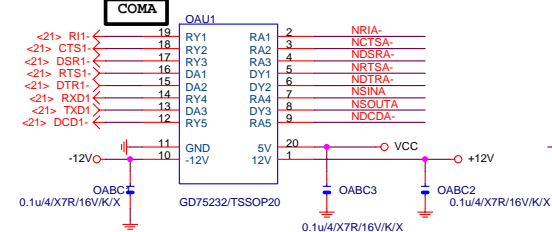
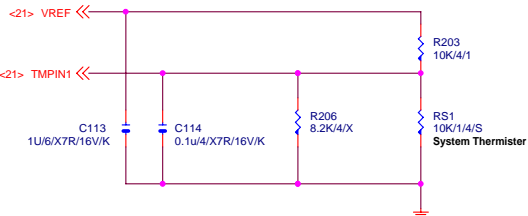
A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7+15P/[11NR6-403004-11]

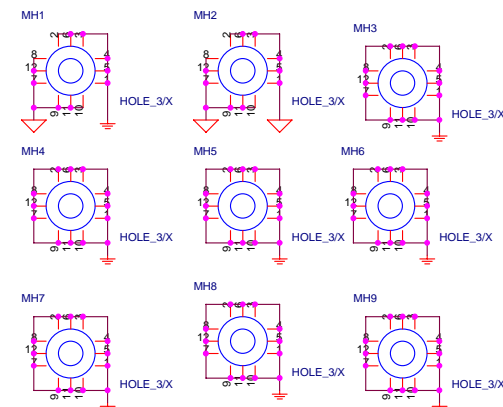
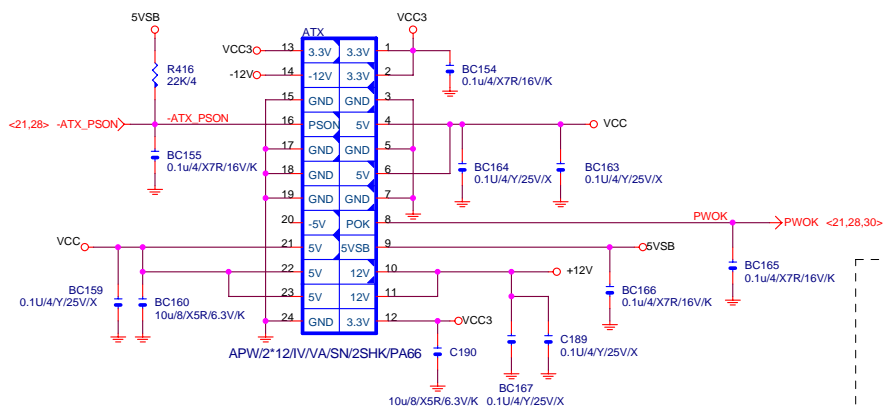
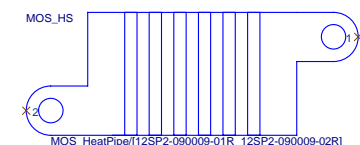
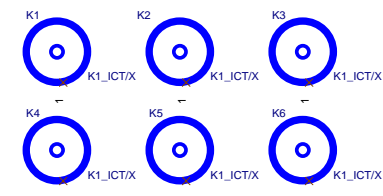
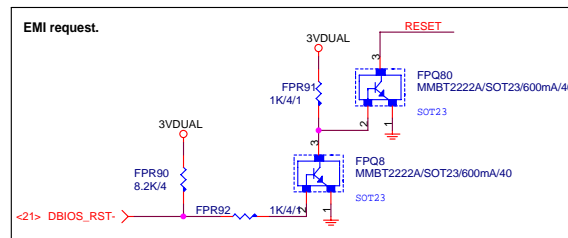
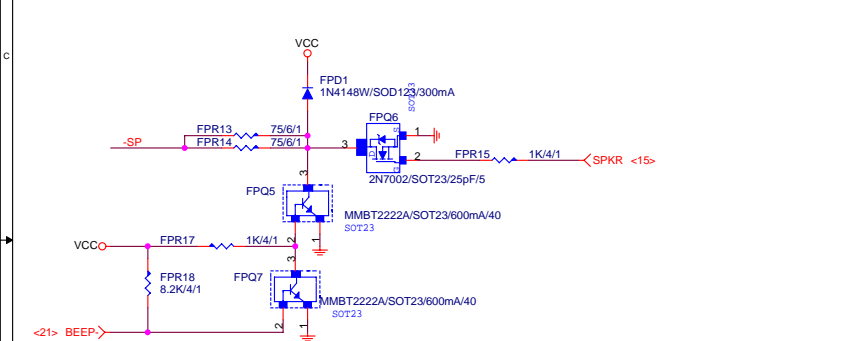
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3R7+15P/[11NR6-403004-31]

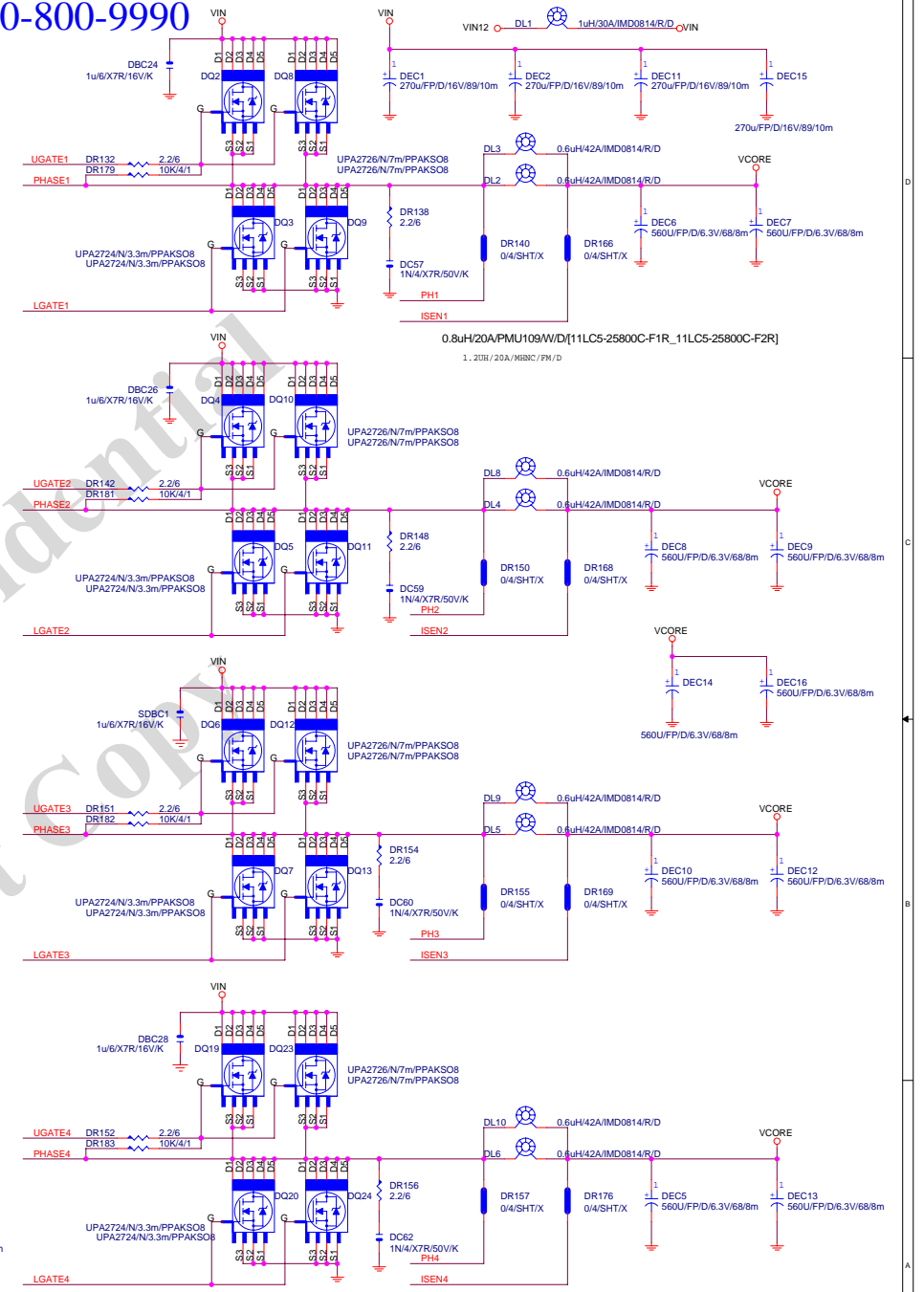
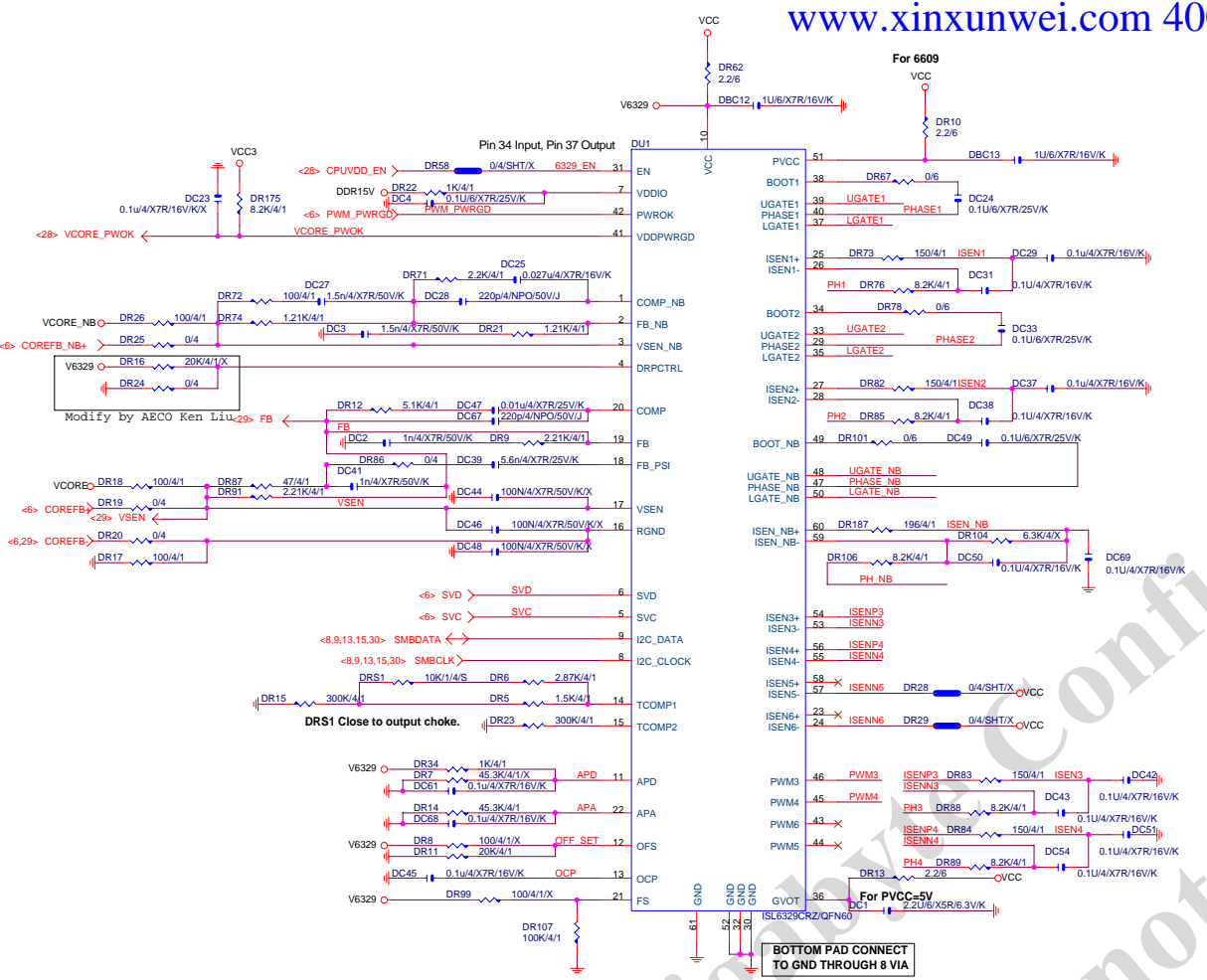
GIGABYTE

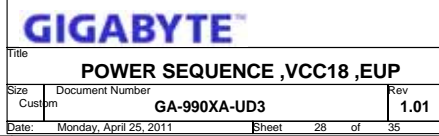
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Size	Document Number	Rev	
Cust	GA-990XA-UD3	1.01	
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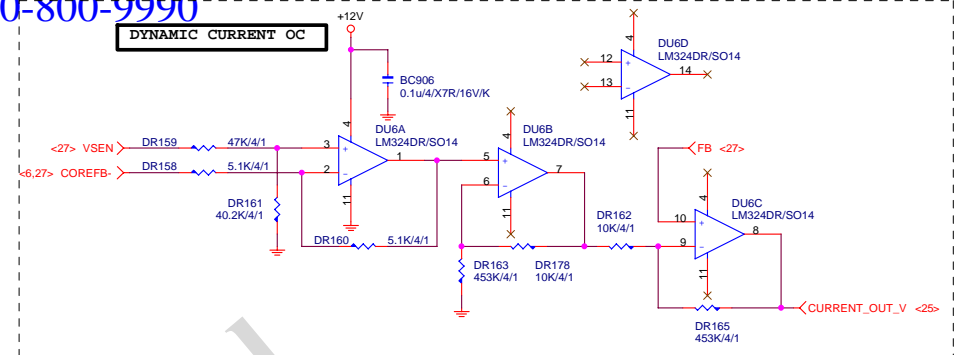
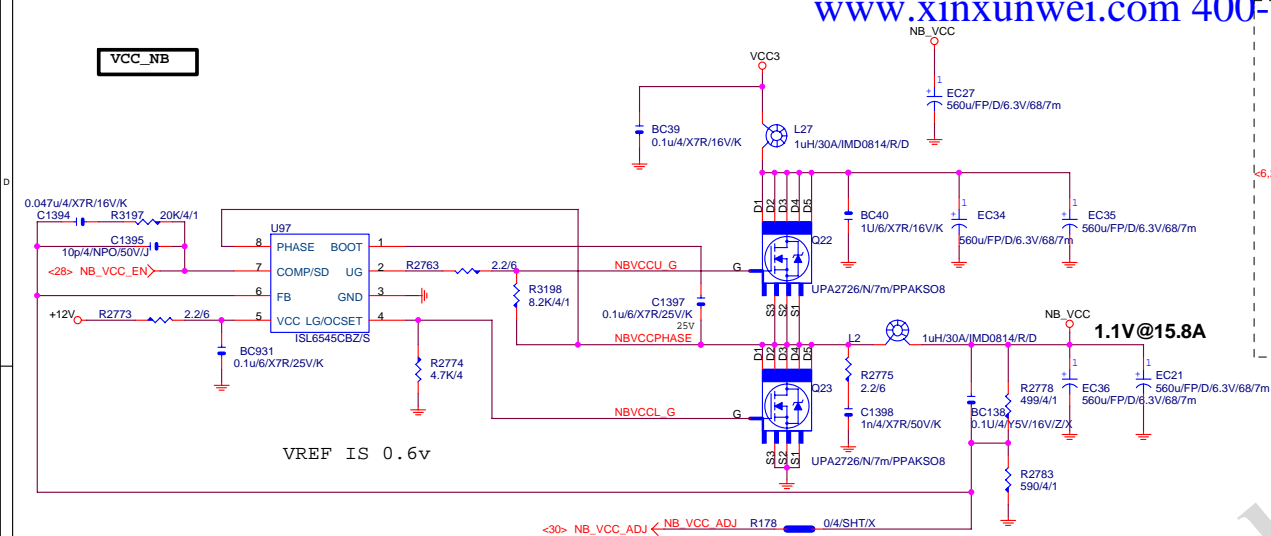
Hardware Monitor circuits





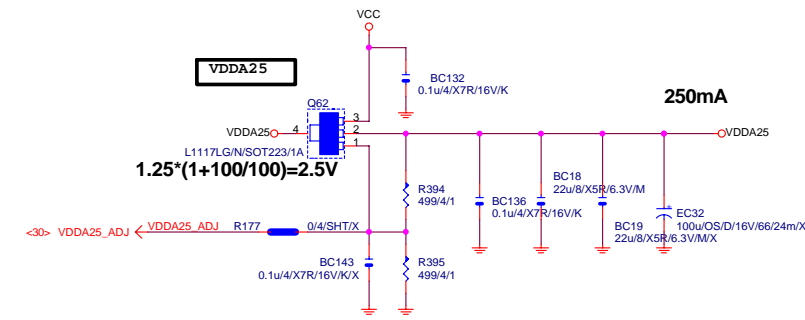
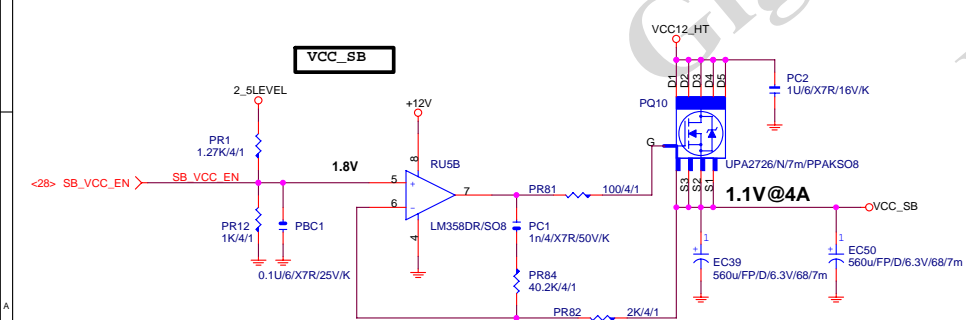
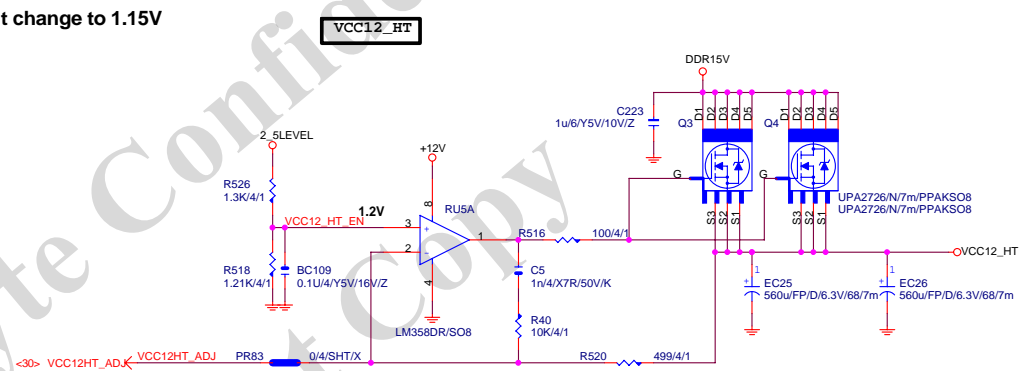
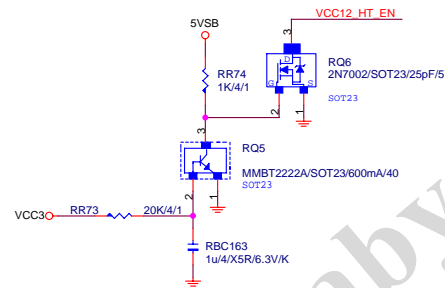






Default change to 1.15V

Patch AMD Validation VDDA25 & VCC12_HT power sequence



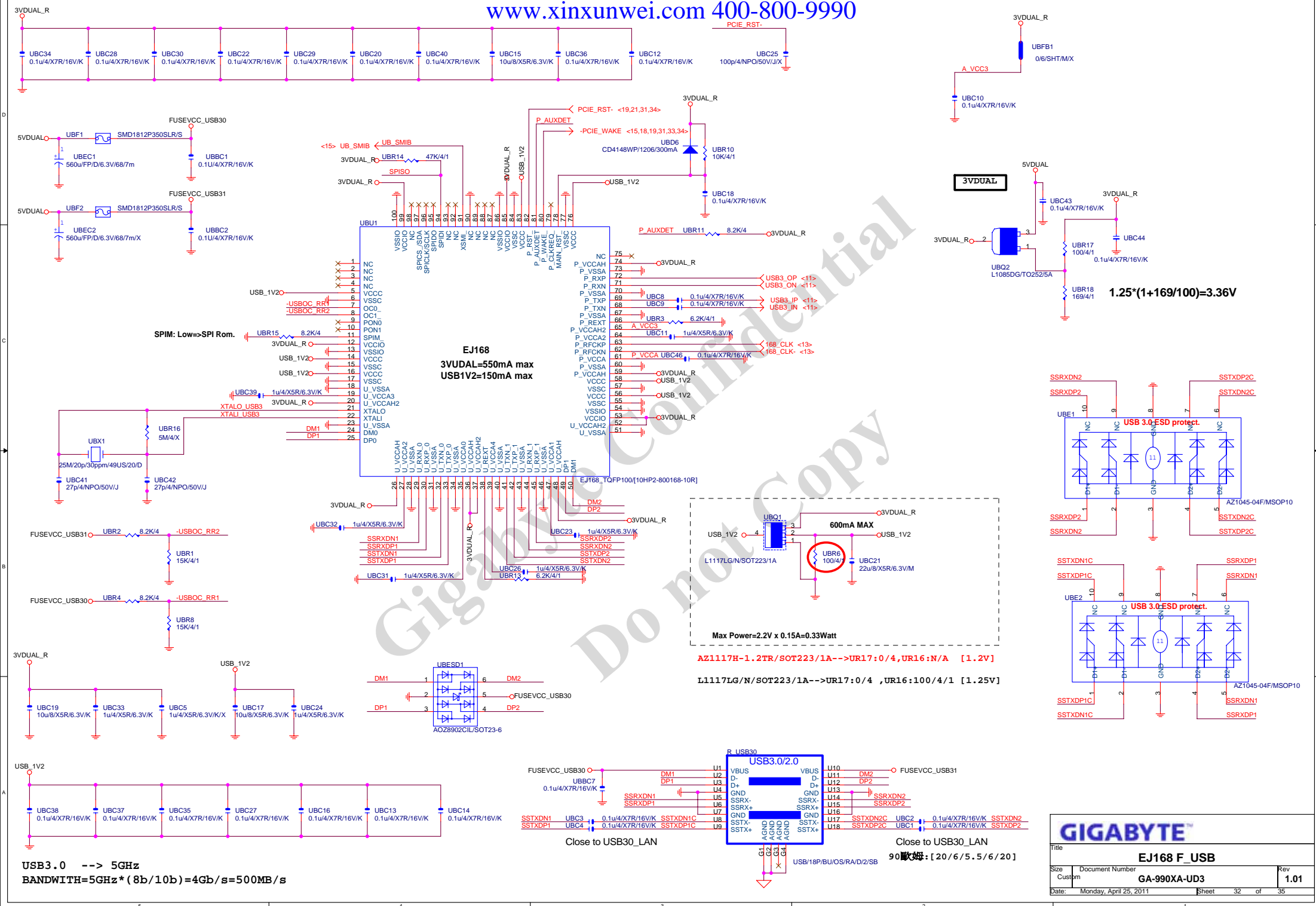


DDR POWER

Rev	1.01
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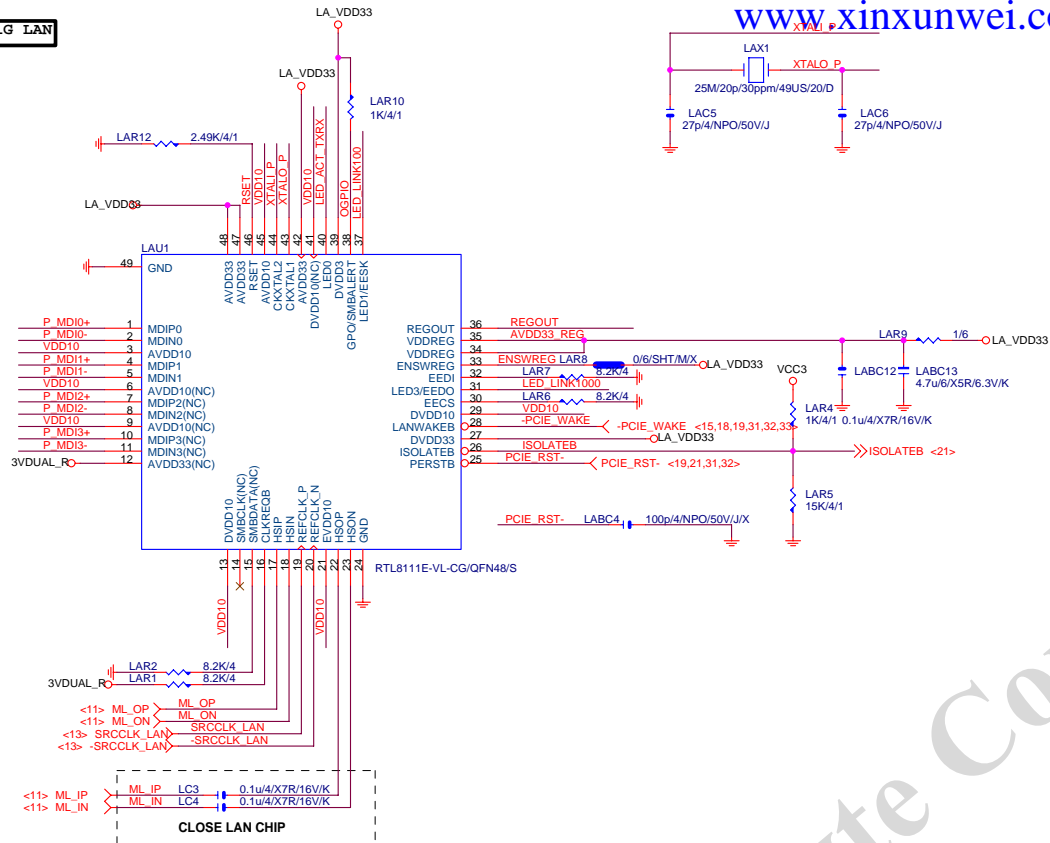
Date: Monday, April 25, 2011 Sheet 30 of 35

[illegible]



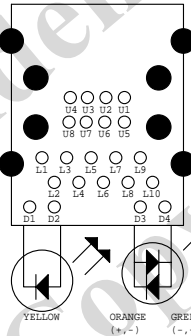


PCIE-1G LAN



USB LAN CONNECTOR

P35-152-19W9

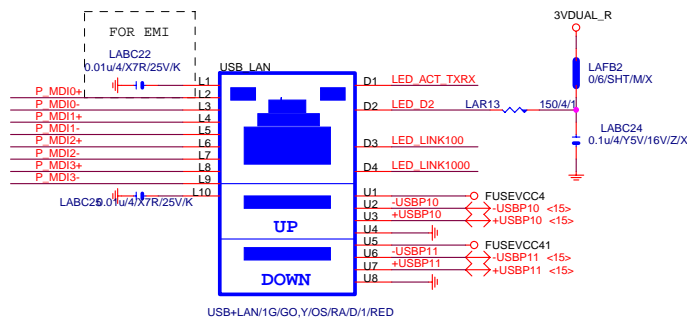


USB LAN

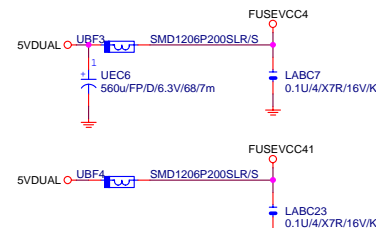
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RTL8111C:LC6-->O

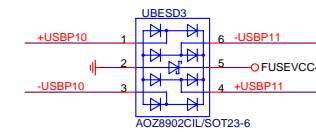
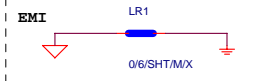
RTL8102E:LC5/LC6-->O



USB+LAN/1G/GO,Y/OS/RA/D/1/RED

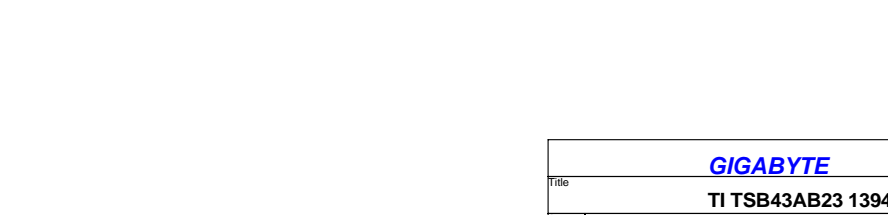
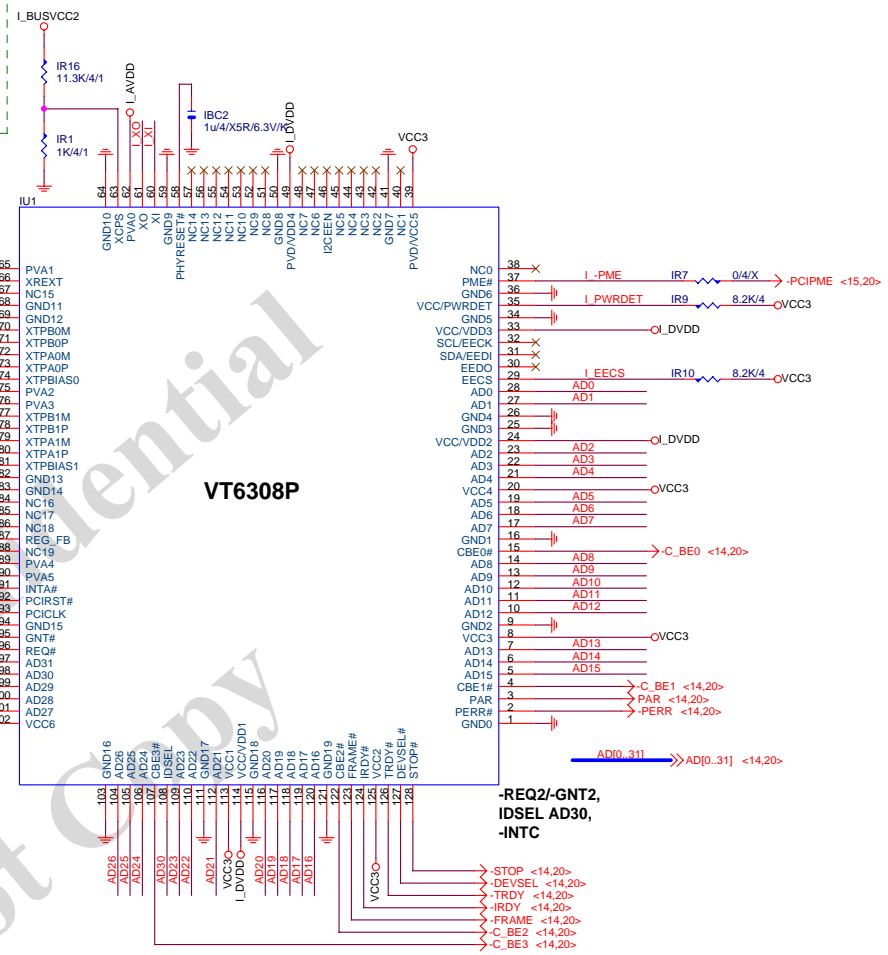
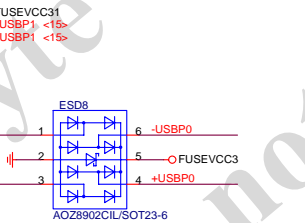
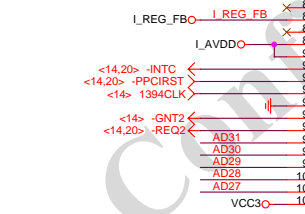
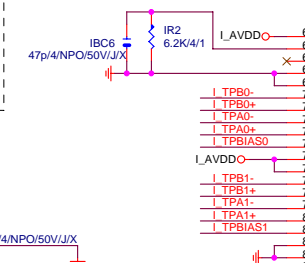
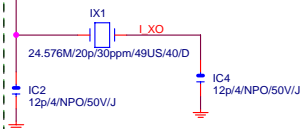
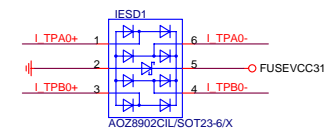
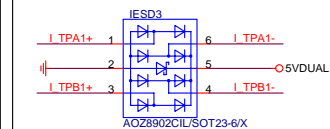
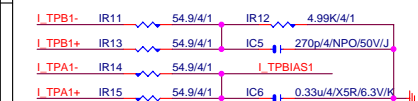
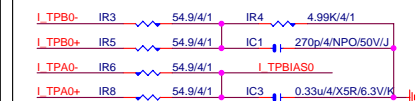
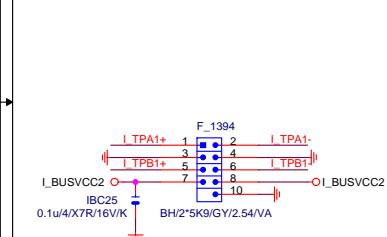
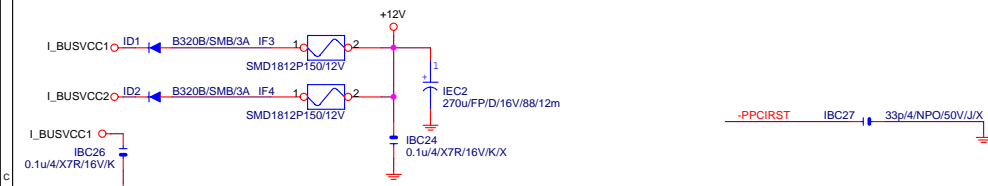
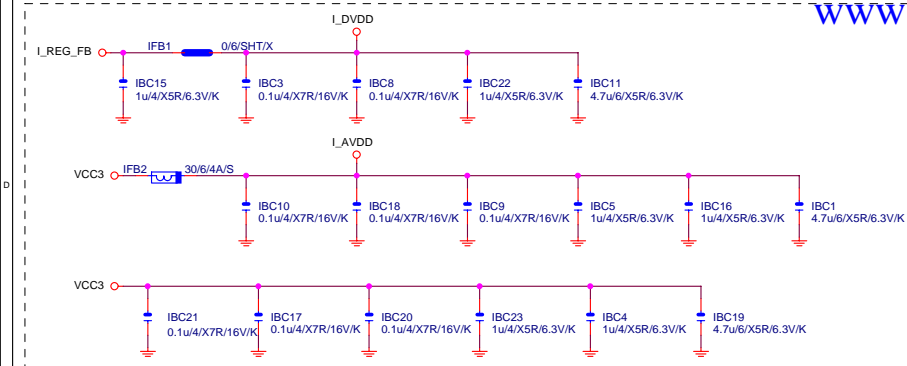


RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

GIGABYTE

Title		
REALTK RTL8111C		
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GIGABYTE

TI TSB43AB23 1394

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